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Amplification of Video Signal Conditioner Circuit Design

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AMPLIFICATION OF VIDEO SIGNALS FROM CID CAMERA BY INCREASING AMPLIFIER GAIN AND BY EXTENDED INTEGRATION

BY

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ABSTRACT

Charge Injection Device (CID) has recently become a popular imaging device due to its versatility and high performance. The UCF's Electro-Optics Laboratory currently uses the TN 2505A, a General Electric solid state CID surveillance camera as an imager in an image processing system. The model offers two useful amplification techniques for video signal under low light condition: electronic gain boost and extended integration. This report describes the design and implementation of an external interface circuit that enables utilization of these two amplification techniques on the TN 2505A.

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INTRODUCTION

For most of todays TV compatible video cameras, the only option available to compensate for low light condition is to open up the lens aperture. For the TN 2505A, GE solid state CID surveillance camera, there are two additional techniques to amplify the video signal. These are: 1) a gain switch to give optional 0 dB, +6 dB or +12 dB electronic amplification, and 2) injection inhibit option to increase integration time which results in proportional amplification. To have access to these options, an external control circuitry is needed. An interfacing circuit was designed, built and tested with the TN 2505A. The development of this interface circuit and how it is used with the TN 2505A in an image processing system is explained in the following chapters.

I. DESCRIPTION OF THE TN 2505A CID CAMERA

A brief description of charge injection device concept and the TV compatible CID camera is helpful in following the development of the interface circuit.

Charge Injection Device Concept

Two basic processes are involved in charge injection devices: charge storage, to convert optical energy into stored electrical charges, and charge injection, to release these stored charges for further electronic processing.

Charge Storage. The basic unit of CID image is an MOS capacitor. Figure 1 illustrates the mechanism of charge storage for an MOS capacitor in an n-type substrate.

By applying a negative voltage to the gate, negative electrons in the substrate migrate toward the ground electrode, creating a potential well near the semiconductor surface which can be exploited for storage of charge.

If a photon with energy greater than the band gap energy is absorbed in the depletion region, a hole and electron pair is created and the free electron will flow through the substrate to the ground electrode while the holes will be stored in the potential well. This charge storage process is used during integration time of CID camera to collect optical information.

Charge Injection. As described above, the application of a gate voltage on an MOS capacitor enables charge storage. By removing this gate voltage, charge injection is activated, as shown in Figure 2, which provides the method of charge read-out. This process is described below.

At the beginning of gate voltage application, a depletion region is formed creating majority carriers, holes in this case, flowing through the potential well. The majority carriers result in a negative current pulse as shown in Figure 3. During integration, photon-generated minority carriers, holes in this case, will be collected at the surface of the semiconductor in the potential well and be stored as shown in Figure 1. Meanwhile, photon-generated majority carriers continuously flows through the substrate, resulting in negative current as shown in the shaded area in Figure 3. At the removal of gate voltage, stored positive charges are injected into the substrate to recombine with electrons, resulting in a positive current which is the combined effects of photon-generated carriers during integration and "gate voltage charge" generated carriers. Integration of consecutive positive and negative current pulses will yield a net signal that is proportional to the the photon-generated charge.

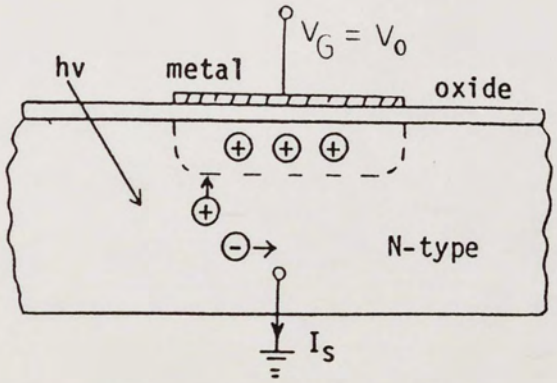


Figure 1. CID Charge Storage Process (Barbe 1975).

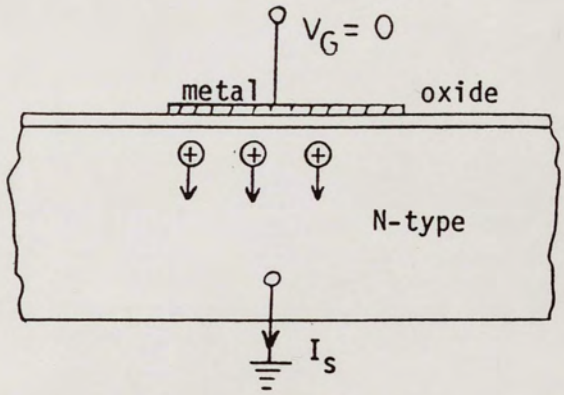


Figure 2. CID Charge Injection Process (Barbe 1975).

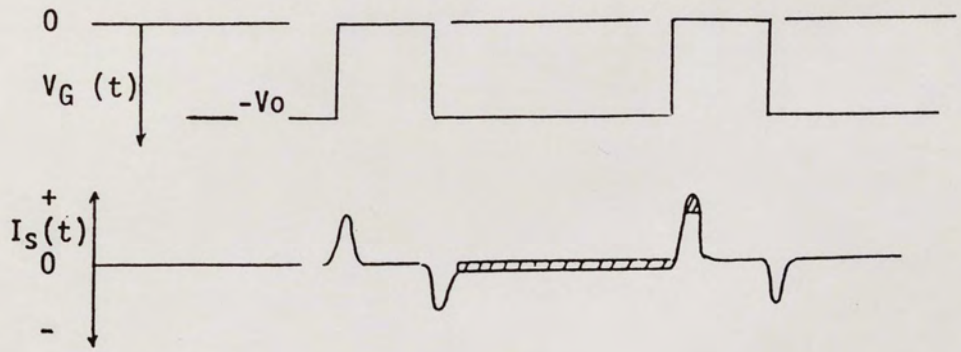
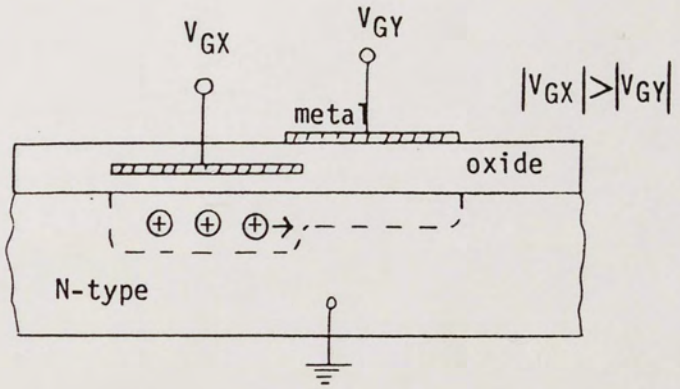
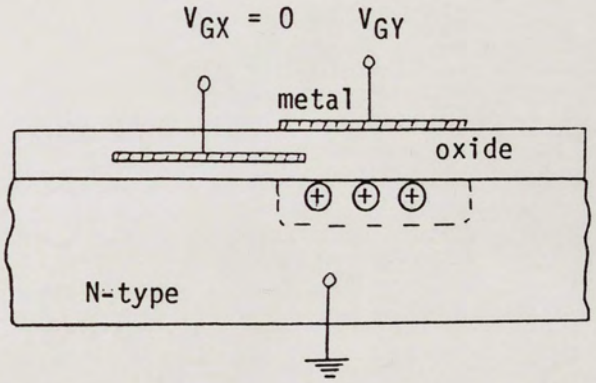


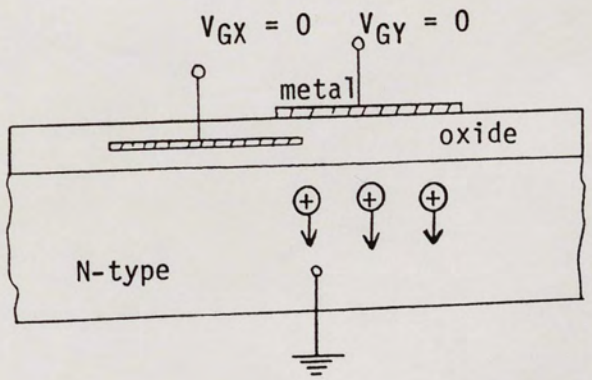
Figure 3. Output Current During Integration and Injection (Barbe 1975).



(a). Charge Storage.



(b). Charge Transfer.



(c). Charge Injection.

Figure 4. Basic Cell of CID Area Array (Barbe 1975).

CID as a Two-Dimensional Imager. For two-dimensional imaging CID arrays, each unit cell requires two separate electrodes for two storage capacitors. One electrode is connected to horizontal access line and the other to a vertical line. Figure 4 shows a normal charge storage injection scheme for a two-dimensional CID imager. As one electrode is turned off, the charges under that electrode is transferred to the other potential well. The stored charges are only injected if both electrodes are turned off. This process provides the basis for random access CID.

The TN 2505A CID Camera

General Information and Theory of Operation. The TN 2505A is compact TV camera with built-in video signal processing, amplification and synchronization to generate a standard RS-170 video output format which may be directly connected to a TV monitor to produce video images. The internal hardware of the TN 2505A comprises of four PC boards: the imager, video, power supply and mother board. Figure 5 illustrates the general operation of the CID camera.

The imager serves as the mounting surface for the CID imager and contains the scan generator LSI (Large Scale Integrated circuit) and the hybrid video pre amplifier. The video board contains the video amplifier LSI and an aperture correction circuit. The power supply board contains the clocking and power supply circuitry. The mother board serves as the interconnection between the boards and external interface.

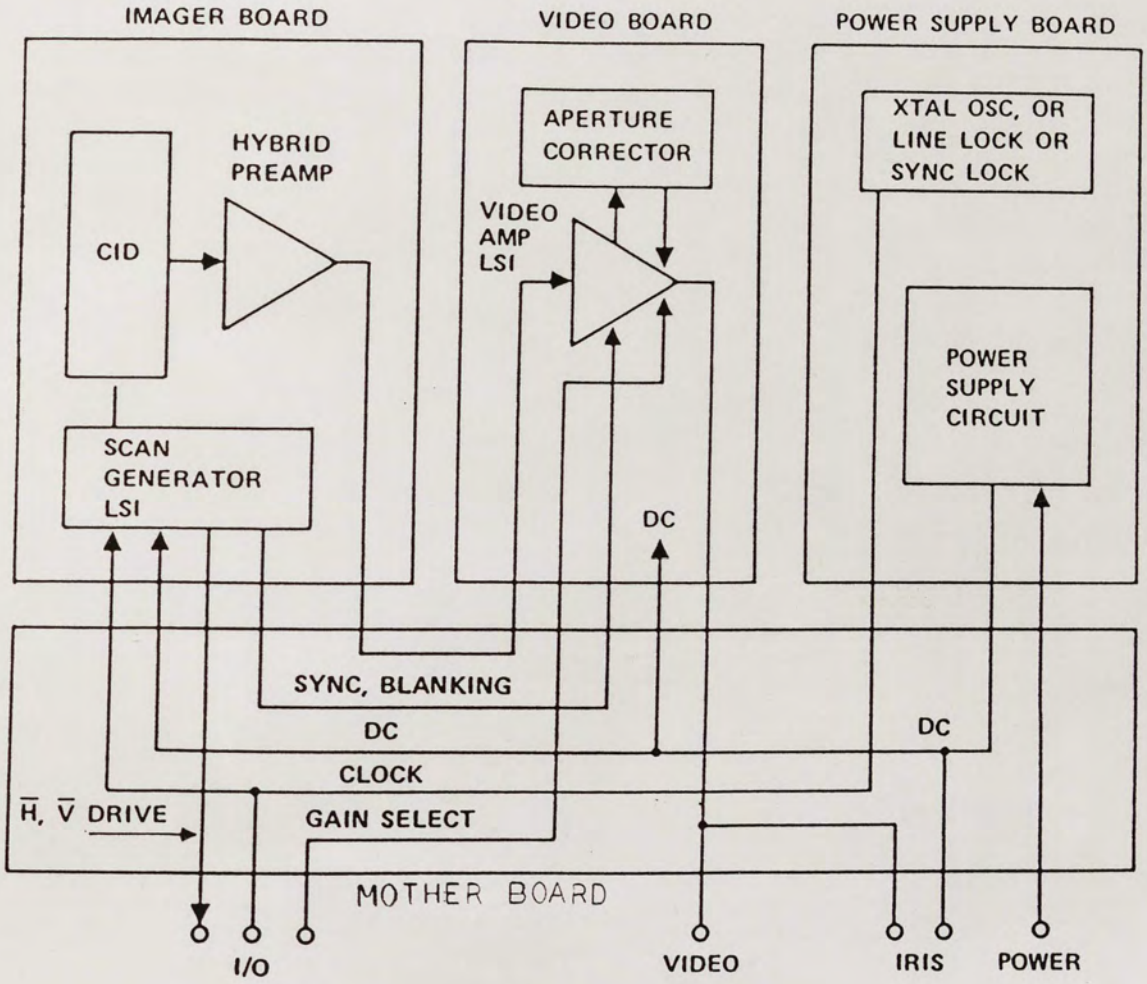


Figure 5. CID Camera Functional Block Diagram

(TN 2505 User's Manual)

Light striking the camera lens is focused onto the CID imager, which stores photon-generated charges as described before. Charge read-out is performed by addressing the individual pixel using X-Y scanning performed by the scan generator LSI. The resulting read-out current is fed in the hybrid pre-amp to produce video output waveform. This waveform is then routed to the video board for amplification and processing, which is mainly the conditioning of the video waveform to conform to RS-170 standard.

The RS-170 Video Output Format

The TN 2505A generates video signals that conforms to the EIA-RS-170 video format specification which employs an interlacing scheme for video image display. Figure 6 illustrates the interlace scanning format.

Video signal representing an image is scanned from left to right and from top to bottom on a monitor. For an interlace format, the series of horizontal lines are divided into even and odd fields. The entire even field is scanned/displayed first, then the entire odd field follows. Each field takes 1/60 second to be completely scanned, and the entire frame is displayed in 1/30 second.

The horizontal scan lines are separated from each other by a horizontal sync pulse. At the occurrence of this pulse, the scanner resets to the left of the field and to the next appropriate horizontal line. The sequence continues until the last line of a field is reached. After the last line of the field is scanned, a vertical pulse, which separates the odd and even fields, is generated and the scan is reset to the top left corner on the scan line of the next field. Figure 7 illustrates an example of the composite RS-170 video signal.

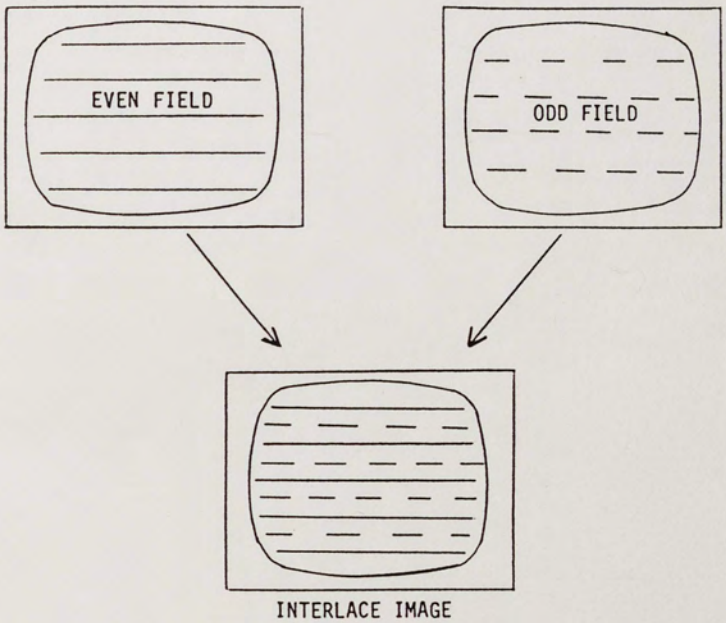


Figure 6. RS-170 Interlacing Scheme

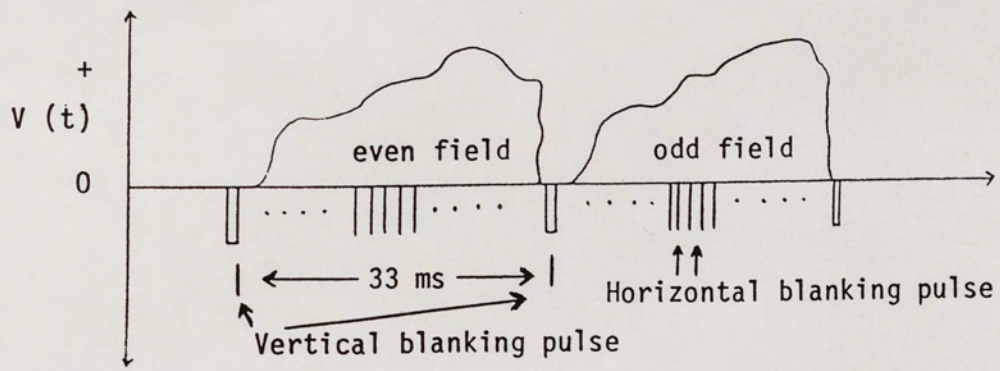


Figure 7. RS-170 Composite Video Signal

Video Amplifications Via I/O Receptacle on TN 2505A

The TN 2505A I/O connector makes available a number of timing signals and mode controls that makes it possible for external interfacing and controlling of the camera operation. These connectors are described below:

Pin	Designation
1	Ground
2	Clock
3	Gain Switch
4	Vertical Drive
5	N/C
6	N/C
7	Injection Inhibit
8	Horizontal Drive
9	+5 Vdc
10	+10 Vdc
11	-5 Vdc
12	Clock Return

Two methods of video signal amplifications on the TN 2505A are available thru the I/O connector: electronic amplification by simply increasing the gain on the video amplifier board and extended integration by increasing the pulse width of CID gate voltage (as described earlier). Pin 3 of the I/O receptacle is designated gain switch, which provides either 0 dB, +6 dB or +12 dB via video amplifier board. Pin 7 is the injection inhibit port, which controls the integration time of the CID imager, hence the amplitude of the output video waveform. The rest of the I/O pin outs provide timing pulses and power levels necessary for the synchronized control of these amplification techniques.

II. INTERFACE CIRCUITRY -- DESIGN AND OPERATION

Design Considerations

a. Gain Switch. Implementation of the gain switch is simple with I/O pin 3. When pin 3 is in the open state, gain switch is at 0 dB. When this pin is connected to +5 Vdc or +10 Vdc levels, the gain is at +6 dB or +12 dB respectively. Since +5 Vdc and +10 Vdc are provided as I/O pin outs, all that is needed to implement this function is a three position switch.

b. Injection Inhibit. At normal state, the Injection Inhibit pin 7 is at +5 Vdc. To activate Injection Inhibit, pin 7 must be pulled down to -5 Vdc. Return pin 7 to +5 Vdc results in the output of one field of video image. The interface circuit for Injection Inhibit is more involved than for the gain switch. Several considerations need to be addressed to successfully implement this function.

o As described in Chapter 1, at the release of gate voltage, the camera immediately outputs one field of video image. In order to synchronize with the frame grabber, the device in the image processing system that stores and process video images, the Injection Inhibit pin must return to its normal +5 Vdc synchronization with a vertical blanking pulse where a new field begins.

o Vertical and horizontal blanking pulses are output from the TN 2505A at MOS levels. These timing pulses need to be shifted to TTL levels to interface with external hardware.

o In order to switch pin 7 between +5 Vdc and -5 Vdc, a buffer circuit is needed.

o In the development of this one-shot circuit, glitches at initial turn on of the Injection Inhibit switch destroy the synchronization between the Injection Inhibit and the vertical blanking pulse. A scheme is needed to eliminate these glitches.

The interface circuit of Figure 8 has addressed all these problems and successfully interfaced with the CID camera to perform video signal amplification.

Interface Circuit Operation

The interface circuitry is broken up into functional areas to simplify circuit operation.

In area A, gain switch pin 3 is connected to +5 Vdc, +10 Vdc or open connection via switch 2 for gains of +6 dB, +12 dB or 0 dB, respectively.

Area B is the level shifting circuit for the horizontal and vertical blanking pulses. Q_1 and Q_2 are depletion-mode MOSFETs which turn on when P1-8 and P1-4 are at +5 Vdc, pulling P2-1 and P2-2 low. These MOSFETs turn off when P1-8 and P1-4 are at -5 Vdc and resistors R_3 and R_4 pull P2-1 and P2-2 up to +5 Vdc. Thus, the circuit shifts the MOS level from the CID to TTL level to be ready for interfacing with other hardware and the computer.

Area C is the circuit which synchronizes Injection Inhibit pulse and the vertical blanking pulse. U1 is a D-flip flop, whose input is selectable via switch 1, between the output of a one-shot circuit or a computer's I/O port. The D-flip flop clock pulse is derived from the TTL level vertical blanking pulse. The synchronized output pulse is fed into the Injection Inhibit buffer.

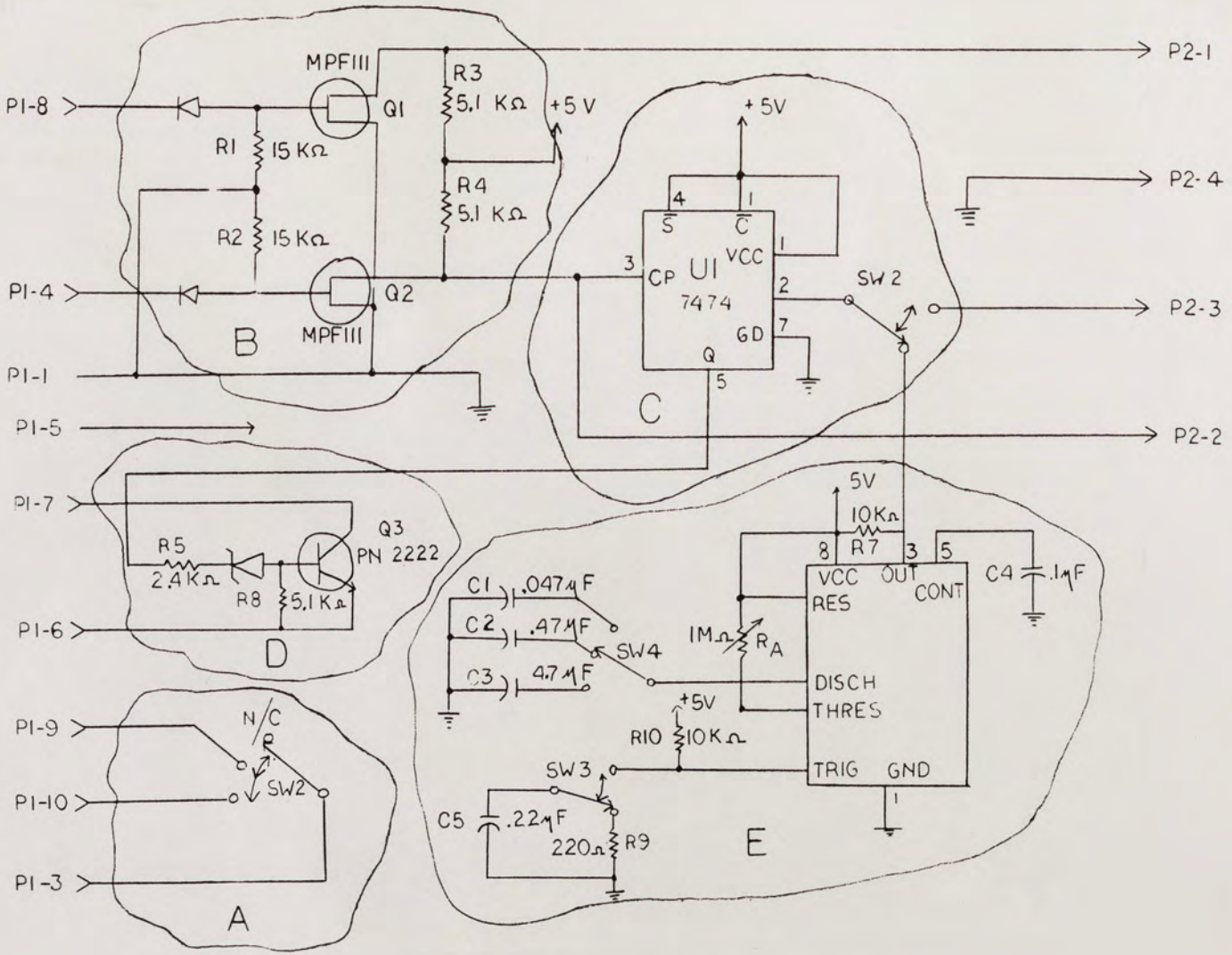


Figure 8. Schematic of CID I/O Interface

Area D is the Injection Inhibit buffer. Q_3 is an N-channel BJT which turns on when output of the D-flip flop is high, pulling pin 7 to -5 Vdc and initiates Injection Inhibit. When the output of the D-flip flop goes low, pin 7 is returned to the +5 Vdc level and the CID camera outputs one field of image.

Area D is the one-shot generator using the popular 555 IC chip which controls the integration time of the CID imager. The one-shot pulse width is controlled by a variable 1 MΩ resistor R_A and any one of the capacitors C_1, C_2 or C_3. These capacitors are selectable by means of switch SW4 and all three of them are needed to produce a dynamic range of the pulse width from 1/60 second to over 5 seconds. A calibrated scale is provided to facilitate the setting of integration pulse width. To initiate the pulse generation, trigger pin 2 of the 555 must pulse low for a time no longer than the output one-shot itself. The RC circuit accompanying switch 3 provides a short, clean, glitch-free low going pulse to successfully trigger the pulse width generator.

Operation of the interface box is simple via 5 top mounted switches. A +5 Vdc power supply is needed to provide power to the interface box via 2 banana jacks. Three-position Gain Switch provides a 0 dB, +5 dB or +12 dB electronic gains. Injection Inhibit Timer used in conjunction with the Timing Multiplier provides calibrated timing pulses with dynamic range from 1/60 second to over 5 seconds. A momentary switch labeled Injected Inhibit Start is used to initiate the one-shot output. An additional Injection Inhibit SW1 provides the option to switch the timing pulse control from the interface box to an I/O receptacle, to be interfaced to a computer I/O port in the future. Figure 9 is a picture of the interface box with all the external controls.

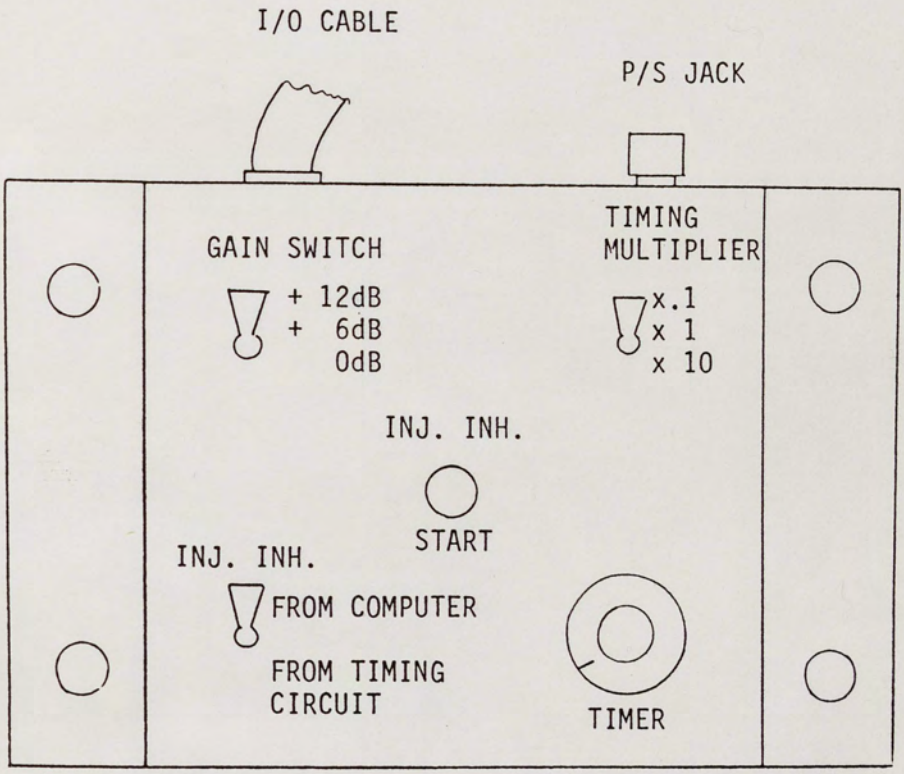


Figure 9. CID Interface Box

III. AN EXAMPLE OF IMPLEMENTATION OF CID INTERFACE BOX IN IMAGE PROCESSING SYSTEM

The CID interface box provides two useful video signal amplification methods under low light condition. In order to demonstrate the implementation of the interface box, the following experiment was performed and contrast and signal-to-noise ratio of video images resulting from these amplification techniques are examined and analyzed.

Experiment Set-Up

To examine the effects of amplification options on the interface box, an image processing system was used to collect and analyze video image data. The image processing system includes the following equipment:

- Intel System 310 Computer
- Panasonic TR 124MA Video Monitor
- GE Model TN 2505A CID Camera
- IP-512-M Image Processing Software
- DC Power Supply
- CID Interface Box

Figure 10 illustrates the set-up of the experiment. A black and white bar chart was used as the object in front of the CID camera. The CID camera collected the object's optical energy and converted it into analog video signals which in turn are digitized by the frame grabber and transferred to the computer. A computer algorithm then analyzed the image for contrast and signal-to-noise ratio.

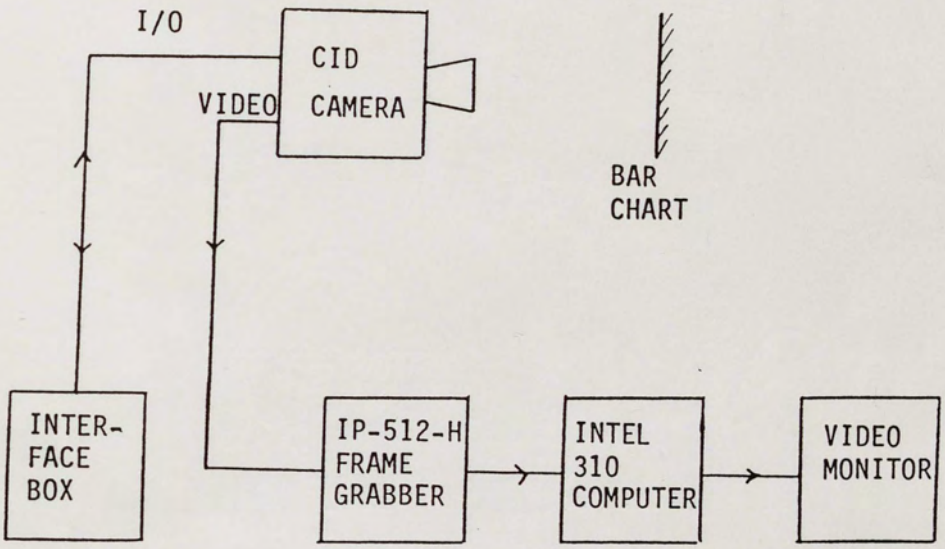


Figure 10. Experiment Set-Up

Procedure

To compare the contrast and signal-to-noise ratio changes using amplifications, the image of the bar chart was taken and analyzed in five different modes: Gain Switch modes 0 dB, +6 dB and +12 dB and Injection Inhibit modes 2-frame integration and 4-frame integration at 0 dB amplifier gain, which are equivalent to +6 dB and +12 dB amplifications, respectively. In each mode, the computer program ANALYZE was used to process the video image and compute the contrast and signal-to-noise ratio. Since the computer does not presently produce hard copy for graphical data, a 35 mm SLR camera was used to take pictures of the processed image graphical results from the video monitor.

Data and Analysis

The data collected below were taken under the following condition:

- CID camera was set at F#/8 with 25 mm lens.
- Video images were taken under existing light condition.
- 35 mm camera was set at F#/8 and 1/15 second.
- The digitized images were sampled at horizontal line number 100. Plots of signal level versus pixel position all had signal level scale from 0 to 200 (255 is the maximum digitized level).

Contrast of the images is derived from the plots to be the difference in average intensities of the white bars and that of the black bars. Noise is the fluctuation within a black or a white bar region.

To compute signal-to-noise ratio, contrast is used to represent signal and the root-mean-square value of the fluctuation within a black or white bar region represents noise.

Computer program ANALYZE sampled the images at vertical pixel line number 100 and plotted Intensity versus pixel position. Average intensity within a black or white bar is computed on horizontal pixel line numbers 60 and 100 respectively. Variance, which is used to derive noise, was computed from the fluctuation in intensity on the horizontal pixel line 60. Figure 11 illustrates the data taking scheme of program ANALYZE. Figure 12 is a summary of data taken in this experiment. Table 1 consolidates data and results outputed from program ANALYZE.

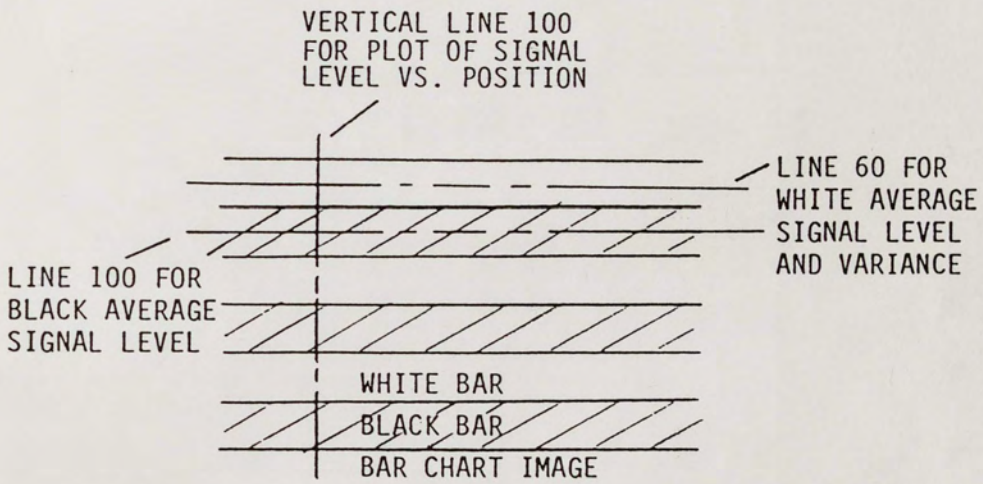


Figure 11. Data Taking Scheme for SNR

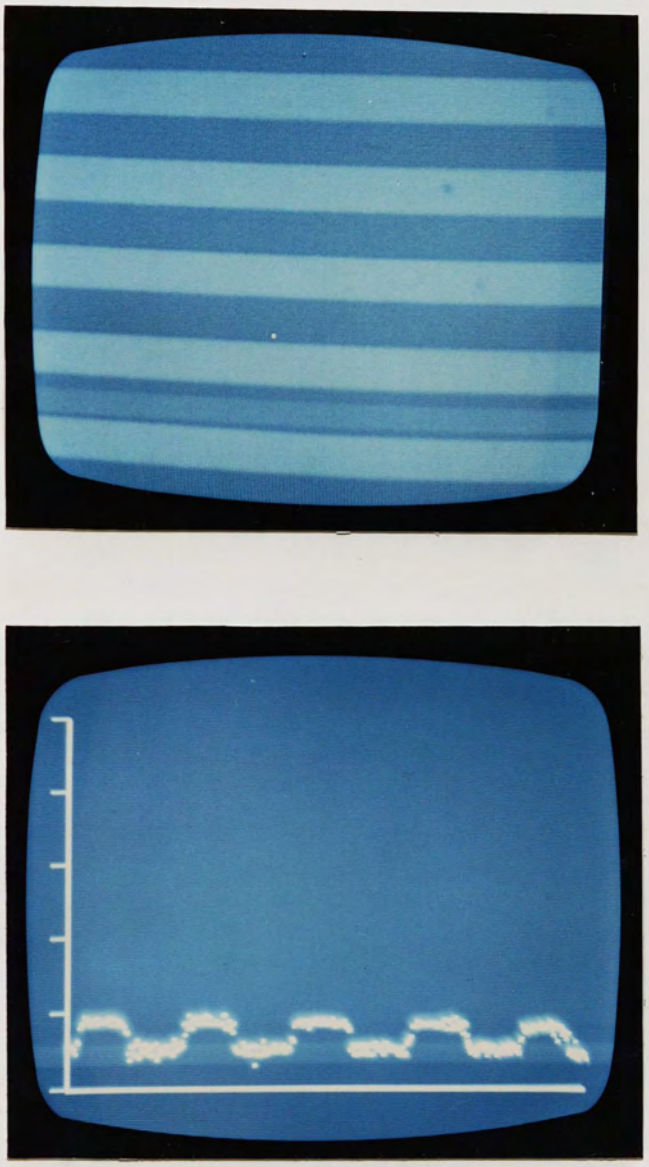


Figure 12a. - Image and Plot of Signal Level vs. Pixel Position at 0 dB

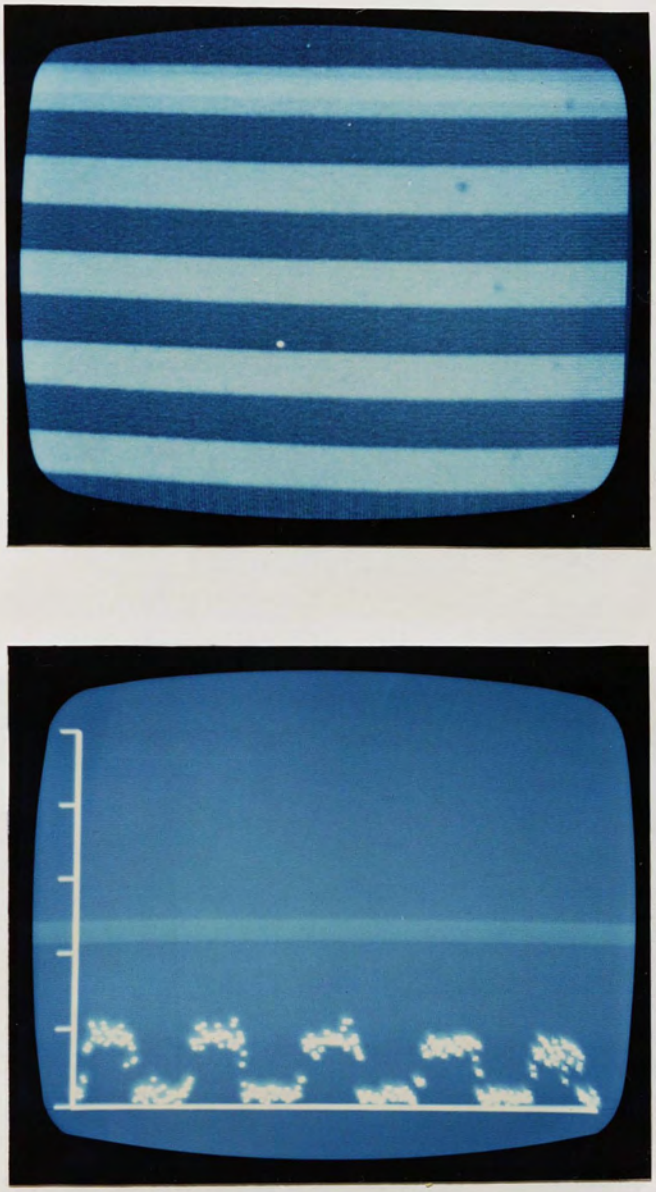
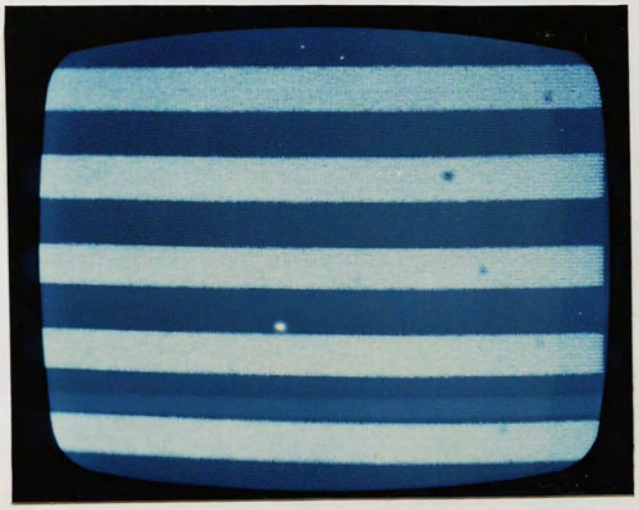


Figure 12b. - Image and Plot of Signal Level vs. Pixel Position at 6 dB



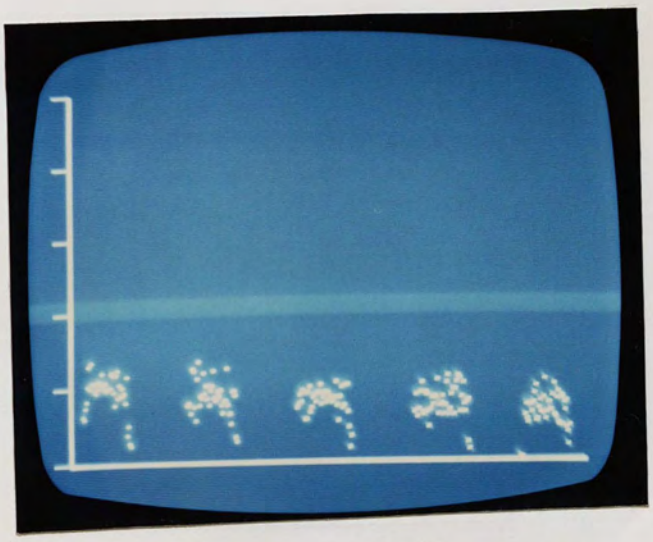
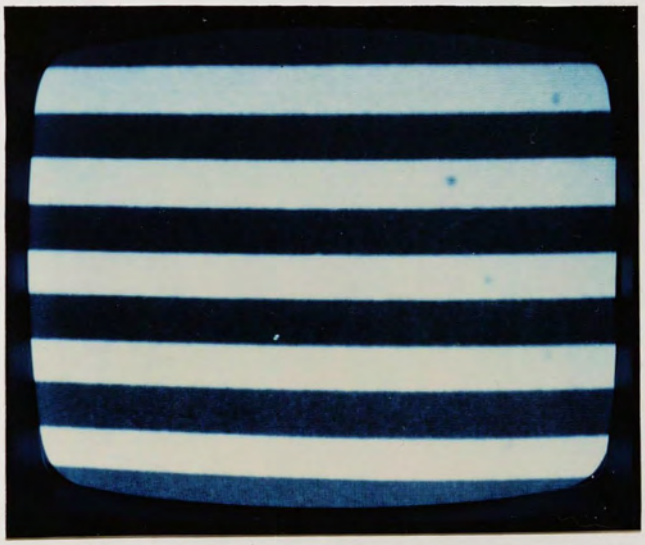


Figure 12c. - Image and Plot of Signal Level vs. Pixel Position at 12 dB



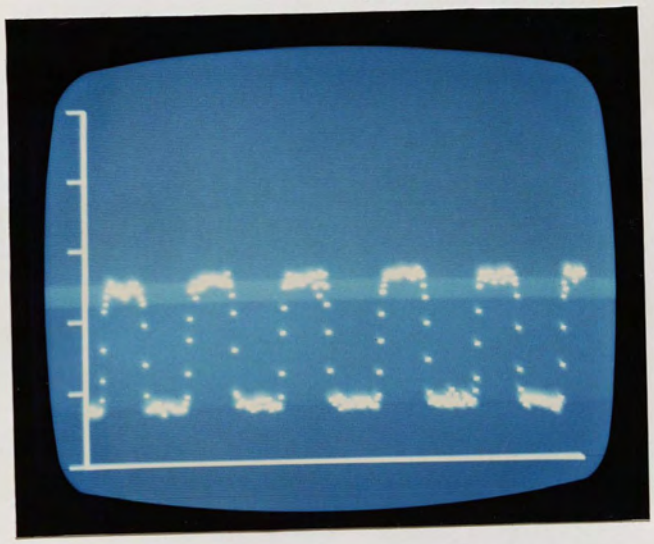
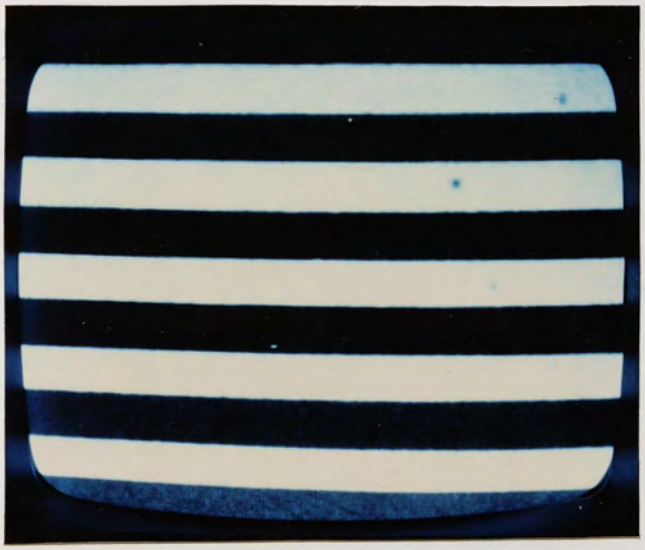


Figure 12d. - Image and Plot of Signal Level vs. Pixel Position at 2-Frame Integration



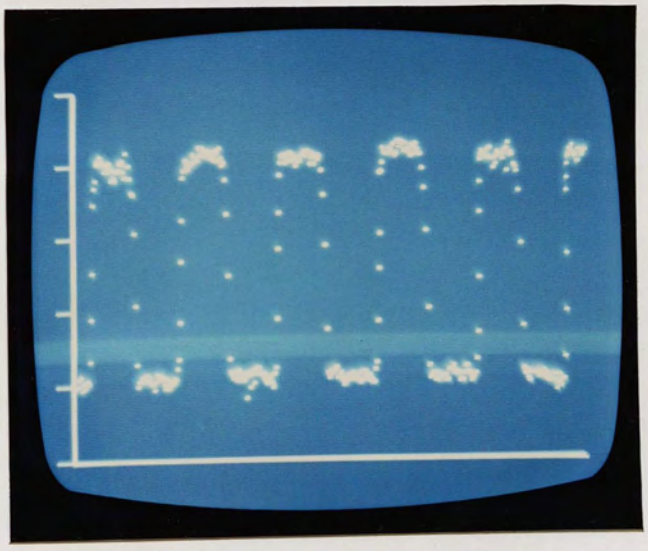


Figure 12e. - Image and Plot of Signal Level vs. Pixel Position at 4-Frame Integration

TABLE 1
DATA AND RESULTS

AMPLIFICATION	AVG. SIG. LEV. ON HOR. LINE 60 (A)	AVG. SIG. LEV. ON HOR. LINE 60 (B)	VAR. SIG. LEV. LINE 60 (C)	SNR $(A-B)\sqrt{C}$
0 dB	35	21	2	9.90
Gain Switch +6 dB	37	5	12	9.24
Gain Switch +12 dB	45	0	60	5.8
Injection Inhibit 2-Frame	100	12	18	20.7
Injection Inhibit 4-Frame	182	42	23	29.2

Results and Interpretation

Dominant noise sources in charge injection devices are shot noise, dark current noise, amplifier noise and fixed pattern noise.

Shot noise is fluctuation of signal due to the random arrival of photons. Approximated by Poisson process, this noise is equated to the square root of the mean number of photons. Expressed in number of carriers, this noise is:

$$[2G^2 \eta EpAdTi]^{\frac{1}{2}}$$

where, G = the photon conductive gain

η = quantum efficiency

Ep = photon irradiance

Ad = pixel area

Ti = integration time

Gain Switch amplification has no effect on SNR as far as shot noise is concern. However, amplification by Injection Inhibit increases SNR due to the fact that in the shot-noise limited case, SNR equals to the square root of the mean number of carriers.

Dark current noise is associated with carriers that are thermally generated to bring the potential well into thermal equilibrium. In terms of the numbers of carriers, this noise is:

$$\frac{Jd\ Ad\ Ti}{q}^{\frac{1}{2}}$$

where, Jd = dark current density

Ti = integration time

Again, Gain Switch amplification has no effect on SNR, theoretically. Injection Inhibit amplification, however, introduces additional dark current noise that becomes critical with long integration time; especially at high temperature where Jd is large.

Fixed pattern noise arises from variation in responsivity across the imager array. Fixed pattern noise represents a noise level common to both Gain Switch and Injection Inhibit amplifications. This noise, however, may be compensated using the well known storage and subtraction technique.

Amplifier noise is post-detector noise for which Injection Inhibit amplification has no effect on SNR. Gain Switch amplification, however, introduces amplifier noise which increases with gain and therefore degrades SNR.

From the above discussion on various noise sources and their effects on SNR using Gain Switch and Injection Inhibit amplification, the following conclusions is drawn:

- Amplification using Gain Switch may increase contrast, or signal, but also noises. SNR therefore, degrades with higher amplification.

- Amplification using Injection Inhibit improves SNR in the case of shot-noise limited. So long as dark current noise is small and integration time is much shorter than is required to saturate CID potential well, this is usually the case.

The results of the experiment in Table 1 supports the conclusion in the above discussion. Both signal-to-noise ratio and contrast are improved with longer integration time. For the cases of Gain Switch amplification, only contrast improves with gain while SNR degrades.

VI. CONCLUSION

The CID interface box provides a means of amplification of video signal useful in low light level imaging. Used in an image processing system, this device provides a simple method to improve contrast and signal-to-noise ration of an image.

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